38. (New) The bus system according to claim 20, wherein the processing unit includes a plurality of re-programmable, dynamically reconfigurable cells.

Remarks

I. INTRODUCTION

Claims 35-38 have been added. Thus, claims 19-35 are now pending in the present application. The drawings, the specification and the abstract have been amended to correct minor informalities. Claims 19, 20, 23, 28 and 30-34 have been amended to more clearly define the subject matter recited therein. No new matter has been added.

The Examiner has objected to the abstract, the drawings, the specification and the claims due to certain informalities. Claims 19 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,113,498 to Evan et al. (the "Evan '498 patent"). Claims 21-27, 30 and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Evan '498 patent in view of common knowledge in the art. Claims 28, 29 and 31-33 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

In view of the following remarks, it is respectfully submitted that all of the pending claims are in condition for allowance. Reconsideration of the present application is requested.

II. CLAIMS 28, 29 AND 31-33

Applicants gratefully acknowledge the Examiner's indication that claims 28, 29 and 31-33 include allowable subject matter. Claims 28 and 31-33 have been amended to be in independent form, and to clarify the subject matter recited therein. Claim 29, which depends from claim 28, has been amended to clarify the subject matter recited therein. It is respectfully submitted that claims 28, 29 and 31-33 are in condition for allowance.

III. OBJECTION TO THE ABSTRACT

The Examiner has objected to the abstract because it is less than 50 words. Applicants have amended the abstract to replace it with an abstract longer than 50 words. Withdrawal of the objection to the abstract is requested.

IV. OBJECTION TO THE DRAWINGS

The Examiner has objected to the drawings under 37 C.F.R. § 1.84(o) because the Examiner believes that the boxes/blocks in the drawings should have suitable descriptive legends. Withdrawal of the object to the drawings is, therefore, requested.

V. OBJECTION TO THE SPECIFICATION

The Examiner has objected to the specification due to certain informalities. As the Examiner will ascertain, the specification has been amended to correct the informalities. Withdrawal of the objection to the specification is, thus, requested.

VI. OBJECTION TO THE CLAIMS

The Examiner has objected to claim 34 because claim 34 recites abbreviations without defining the abbreviations. Claim 34 has been amended in the manner suggested to the Examiner.

The Examiner has also objected to unspecified other claims due to grammatical errors and antecedent basis problems. As the Examiner will ascertain, the claims have been amended to more clearly define the subject matter recited therein.

In view of the foregoing, withdrawal of the objection to the claims is requested.

VII. REJECTION OF CLAIMS 19 AND 20 AS ANTICIPATED BY THE EVAN '498 PATENT

Claims 19 and 20 stand rejected under 35 U.S.C. § 102(b) as anticipated by the Evan '498 patent. Claim 19 has been amended to more clearly define the subject matter recited therein. Claim 20 has been amended to be in independent form

and to more clearly define the subject matter recited therein.

Claim 19

Claim 19, as amended, recites the following:

> A bus system, comprising:
> a processing unit, the processing unit having a multi-dimensional programmable cell architecture; and
> a plurality of individual lines positioned within the processing unit, the plurality of individual lines being bundled;
> wherein the plurality of individual lines provide communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

The Examiner relies on the Evans '498 patent, and, more specifically, on Fig. 10 of the Evans '498 patent, as the basis of the rejection of claim 19.

Fig. 10 of the Evans '498 patent shows a "cell" (of Fig. 1. Each cell includes a multiprocessor 100, input/output section 107-110, a memory 115 and associated timing circuits (oscillator 112 and timing generator 111). *Col. 17, lines 34-39.* This cell is realized with ordinary integrated circuits. *Col. 17, lines 37-38.* The multiprocessor 100 is a stack oriented processor having fours sets of registers 101, providing inputs to an arithmetic logic unit. *Col. 17, lines 49-51.*

The input/output section of the cell comprises four subsections 107, 108, 109 and 110. *Col. 18, lines 20-21.* Three of these subsections 107, 108 and 109 have leads 103, 104 and 105, respectively, for communication with a network and/or controlling and sensing devices connected to the cell. *Col. 18, lines 21-24.* The remaining subsection 110 has a single select pin 106 which can be used to read in commands such as used to determined the cell's ID. Col. 18, 25-27. The subsection 110 is primarily used for timing and counting.

Fig. 10 shows that the multiprocessor 100 is coupled to the input/output subsections 107, 108, 109 and 110 and also to memory 115 via an AD BUS. Additionally, the multiprocessor is coupled to these units via an MD BUS.

In the rejection of claim 19, the Examiner

apparently equates the multiprocessor 100, input/output subsections 107, 108, 109 and 110, and memory 115, together, to the processing unit having a multi-dimensional cell architecture of claim 19. Additionally, the Examiner apparently equates the AD BUS and the MD bus to the individual lines of claim 19. Respectfully, according to the Evan '498 patent, Fig. 10 illustrates a single cell. See, e.g., col. 2, lines 49-50; Fig. 1, elements 27 and 28. Even if the multiprocessor 100, itself, has a multi-dimensional cell architecture (e.g., Evan et al. describes that the multiprocessor 100 may be fabricated using gate array technology), the AD BUS and the MD BUS to the individual lines are not positioned within the multiprocessor 100. Moreover, even if the single cell shown in Fig. 10 could be equated to Applicants' processing unit having a multi-dimensional cell architecture, it is respectfully submitted that the AD BUS and the MD bus do not appear to be "bundled" in any manner, as recited in claim 19.

For at least the foregoing reasons, it is respectfully submitted that the features of claim 19 are neither taught nor suggested by the Evan '498 patent. Thus, claim 19 is not anticipated (nor rendered obvious) by the Evan '498 patent. Withdrawal of the rejection of claim 19 is, therefore, requested.

Claim 20

Claim 20, as amended, recites the following:

> A bus system, comprising:
> a processing unit, the processing unit having a multi-dimensional programmable cell architecture;
> a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled; and
> at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

As discussed above in connection with claim 19, the Evan '498 patent does not teach or suggest the bundling of individual lines within a processing unit having a multi-dimensional programmable cell architecture.

Moreover, the Evan '498 patent does not teach or suggest at least one interface unit which combines a plurality of individual lines to form a bus system. With respect to the feature, the Examiner has stated that "Evan et al. inherently teaches the 'interface unit combining the plurality of individual lines to form a bus system' in Fig. 10, interface units coupling AD and MD buses.

The Examiner apparently equates whatever circuit couples, for example, the multi-processor 100 to the AD BUS or MD bus, to the interface unit of Applicants' claim 20. Respectfully, nothing within the Evan '498 patent even suggests that the AD BUS or the MD bus is comprised of individual lines within a processing unit having a multi-dimensional programmable cell architecture.

For at least these reasons, it is respectfully submitted that the Evan '498 patent does not anticipate the subject matter of claim 20. Withdrawal of the rejection of claim 20 is requested.

VIII. REJECTION OF CLAIMS 21-27, 30 AND 34 AS OBVIOUS OVER THE EVAN '498 PATENT IN VIEW OF COMMON KNOWLEDGE IN THE ART

Claims 21-27, 30 and 34 stand rejected under 35 U.S.C. § 103 as being obvious over the Evan '498 patent in view of common knowledge in the art. In particular, the Examiner believes that features such as "at least one state machine for controlling the at least one interface unit" would be obvious in the art, and the Examiner has taken "Official Notice" that these features are well known and expected in the art.

As an initial matter, Applicants submit that the features recited in claims 21-27, 30 and 34 are, in fact, not well known, at least in the context of the present invention as recited in the pending claims. For example, according to claim 21, a state machine controls an interface unit. The

Examiner states that "[i]t would be obvious to include the above features such as 'at least one state machine for controlling the at least one interface unit', etc. in the system of Evan et al., because it is an alterative way known in the art to use 'state machine' for providing control signals." Respectfully, it is submitted that while a state machine, in general, may be well known, a state machine is not well known for controlling a interface unit which coupled individual lines in a multi-dimensional programmable cell architecture.

Additionally, with respect to claim 23, an address generator generates addresses for selecting a unit coupled to the bus system. Claim 27 recites a bus master unit slave unit in the context of a multi-dimensional programmable cell architecture. With respect to claim 30, a register indicates whether data is stored in the interface unit. The Examiner has not even addressed these particular specific features.

In accordance with MPEP 2144.03, the Examiner is requested to provide a reference or references supporting all of the features the Examiner believes is "well known." If any of the rejections are, instead, facts within the personal knowledge of the Examiner, the Examiner is requested to support the rejections with an affidavit setting forth the facts upon which the Examiner's rejection is based. See 37 C.F.R. 1.104(d)(2).

Furthermore, each of claims 21-27, 30 and 34 depend, directly or indirectly, from claim 20. Thus the arguments above with respect to claim 20 and the Evan '498 patent apply equally to claims 21-27, 30 and 34. The subject matter to which the Examiner has taken Official Notice does not cure the deficiencies of the Evan '498 patent.

In view of the foregoing, it is submitted that claims 21-27, 30 and 34 are in condition for allowance. Withdrawal of the rejection of claims 21-27, 30 and 34 is requested.

IX. NEW CLAIMS

New claims 35-38 recite further features of the

present invention. Each of claims 35-38 depend from one of claims 19 and 20. Thus, each of these claims are patentable over the cited art for at least the reasons discussed above. Additionally, the further features recited in these claims are also not taught or suggested by the cited references.

X. CONCLUSION

In light of the foregoing, Applicants respectfully submit that all pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

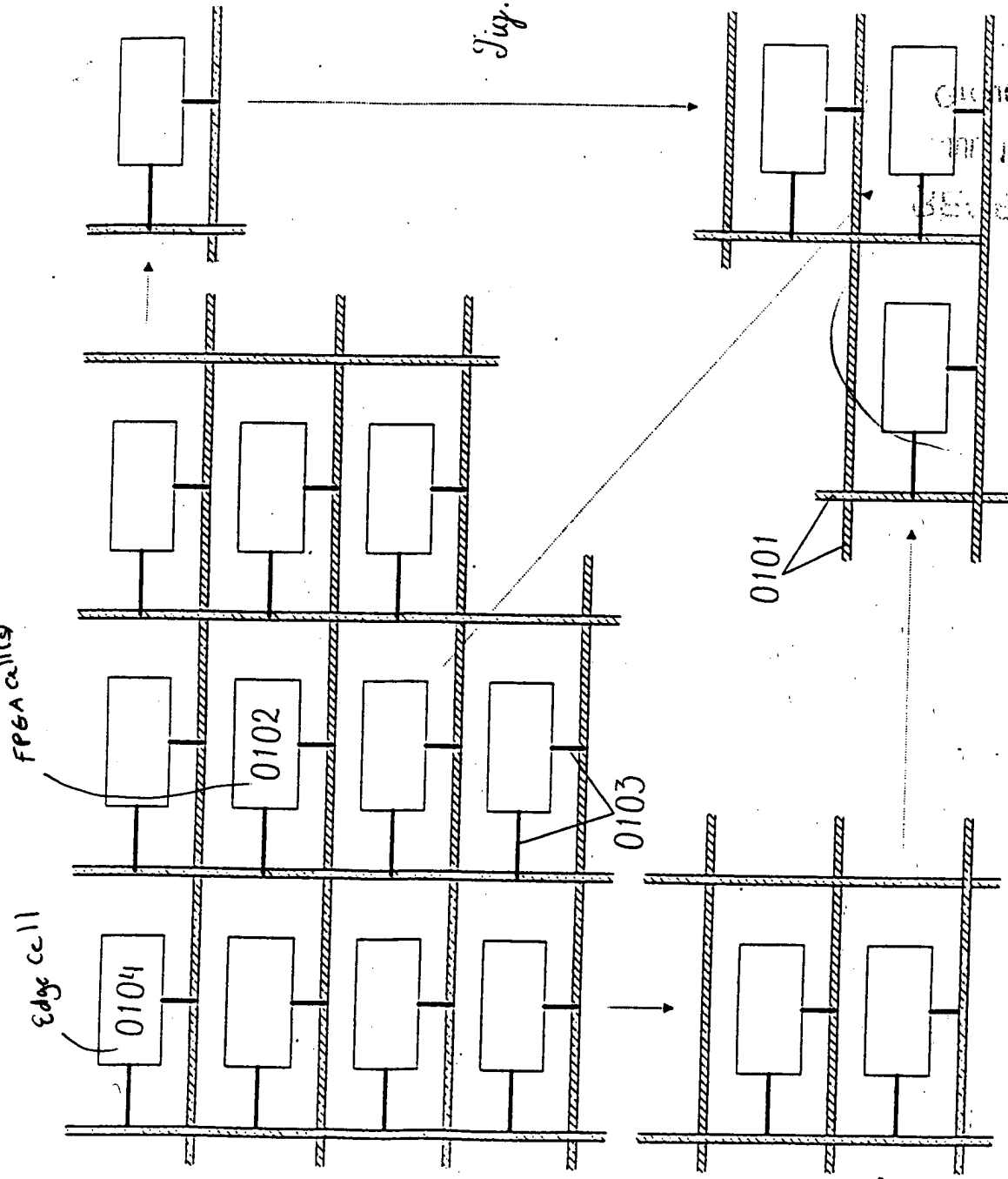
Dated: 29 June 1999

By: _____

Michelle M. Carniaux
(Reg. No. 36,098)

KENYON & KENYON
One Broadway
New York, New York 10004
(212) 425-7200

Fig. 1



The changes to the drawings have been approved by the examiner.
GCP
7/19/99

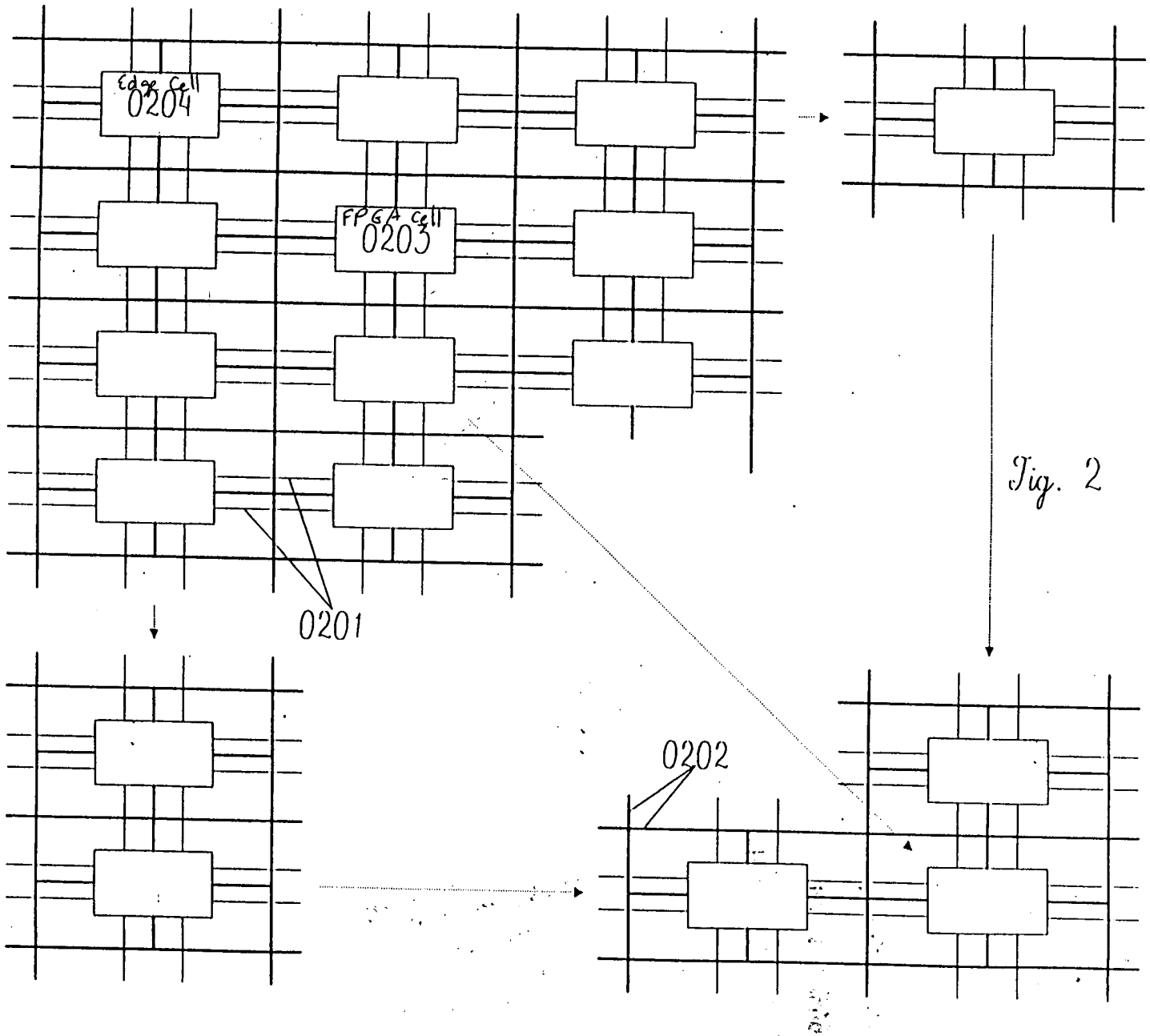


Fig. 2

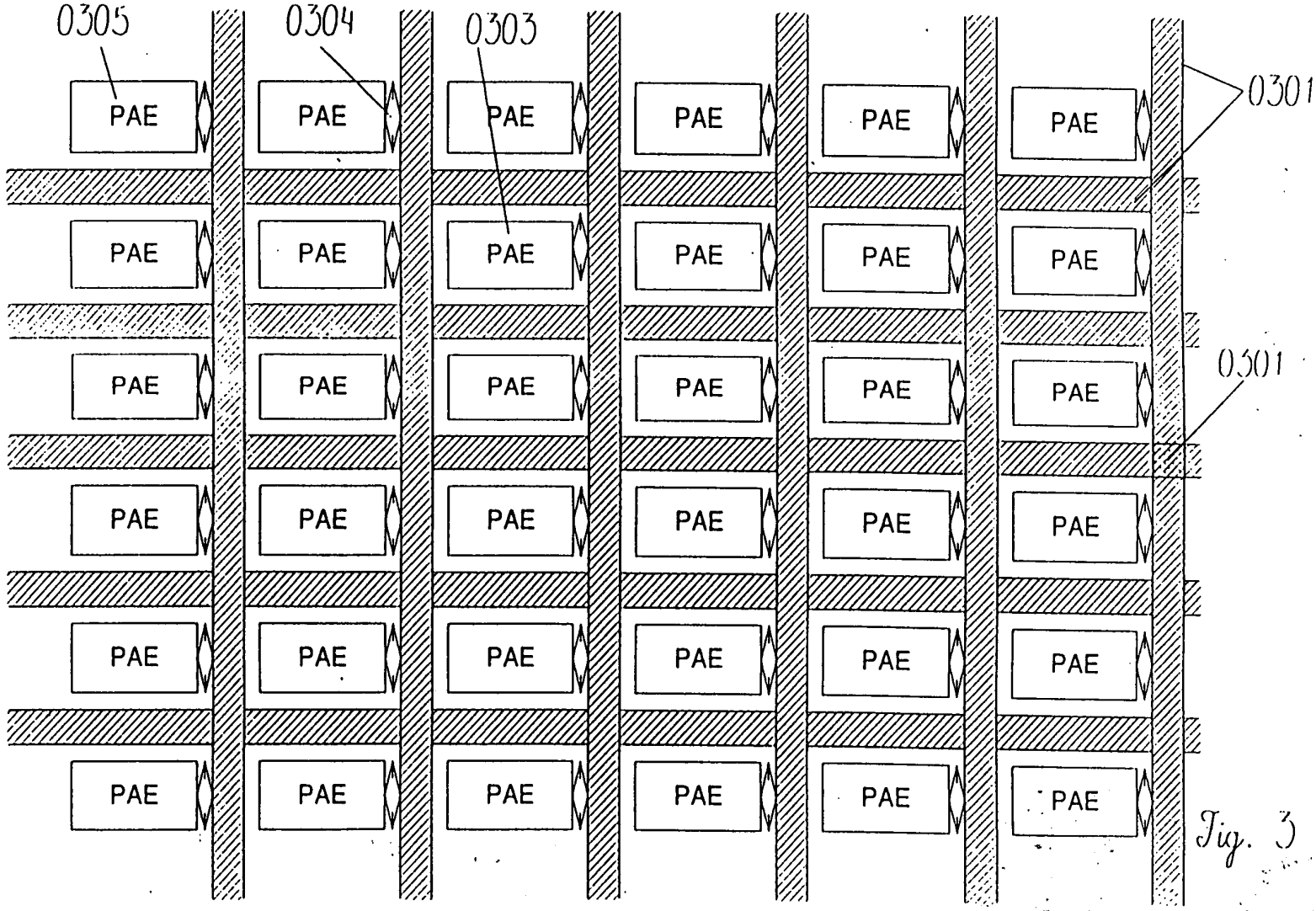


Fig. 3

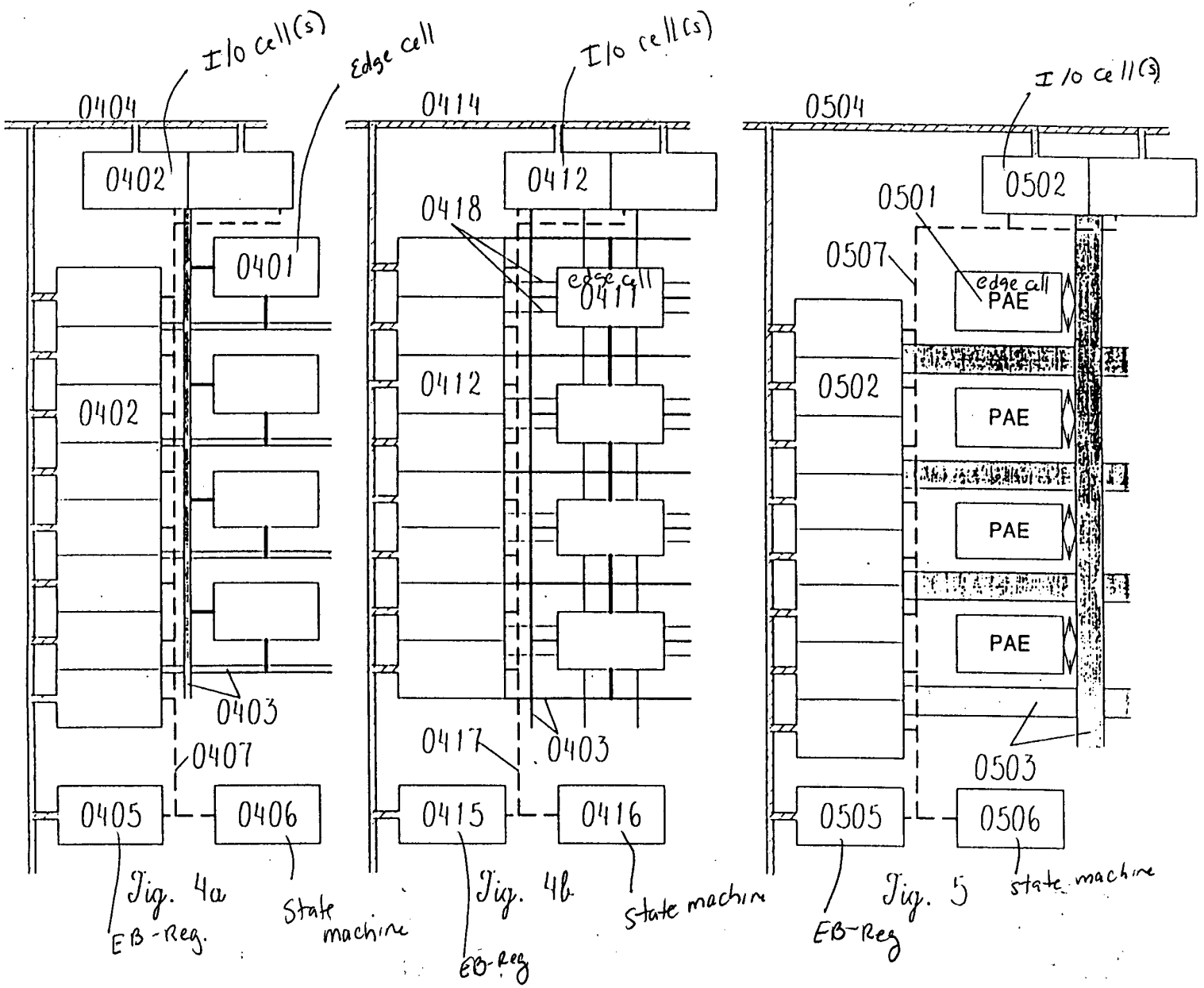
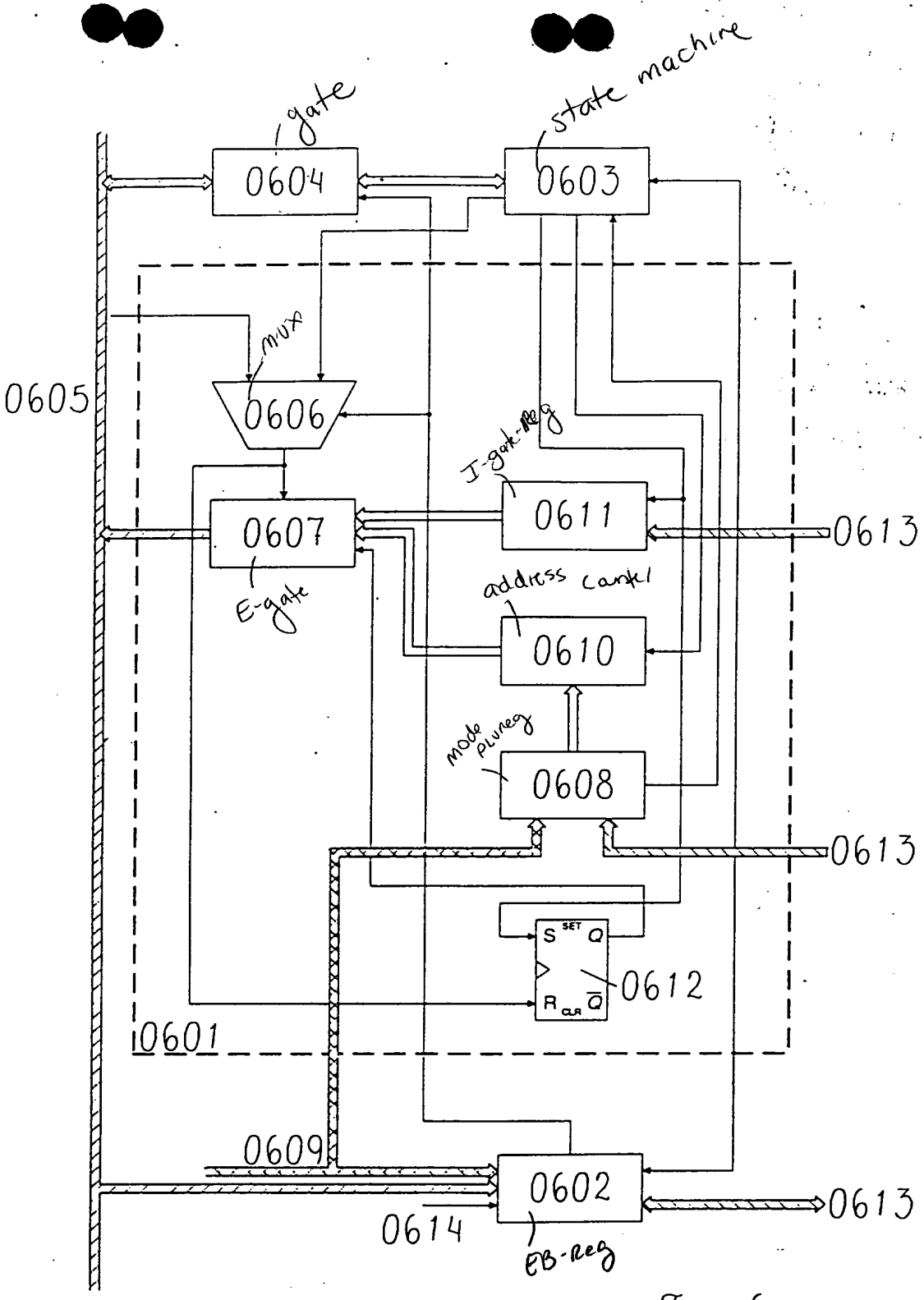


Fig. 4a

Fig. 4b

Fig. 5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0603
0605
MUX
0606
J-gate-Reg
0611
0613
0607
E-gate
address cantrl
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0613
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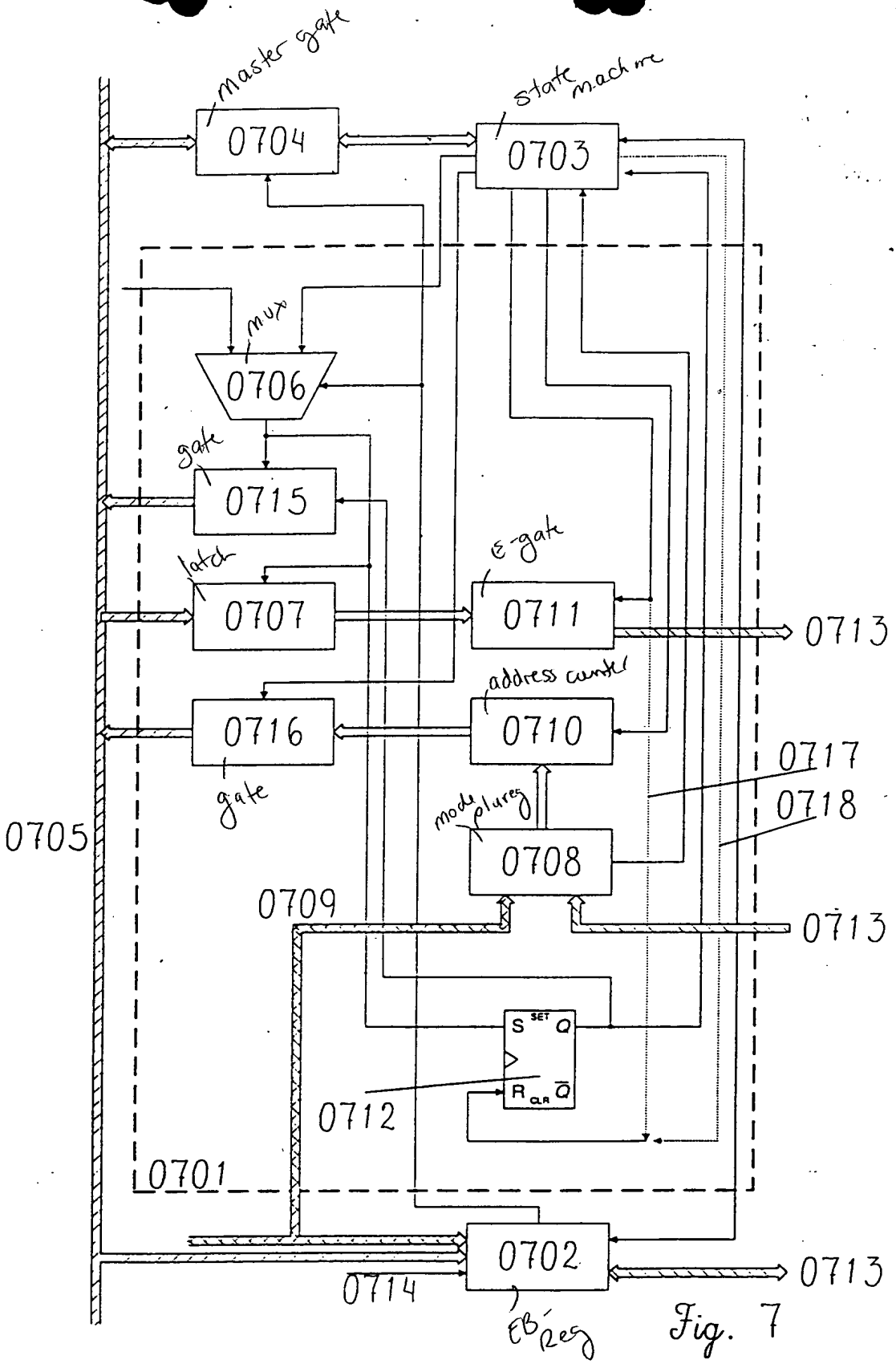
0601
0609
0602
0613
0614
EB-Reg

Fig. 6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mux
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gate
0715
latch
0707
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0713
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0710
0717
0718
gate
mode flipflop
0705
0708
0709
0713
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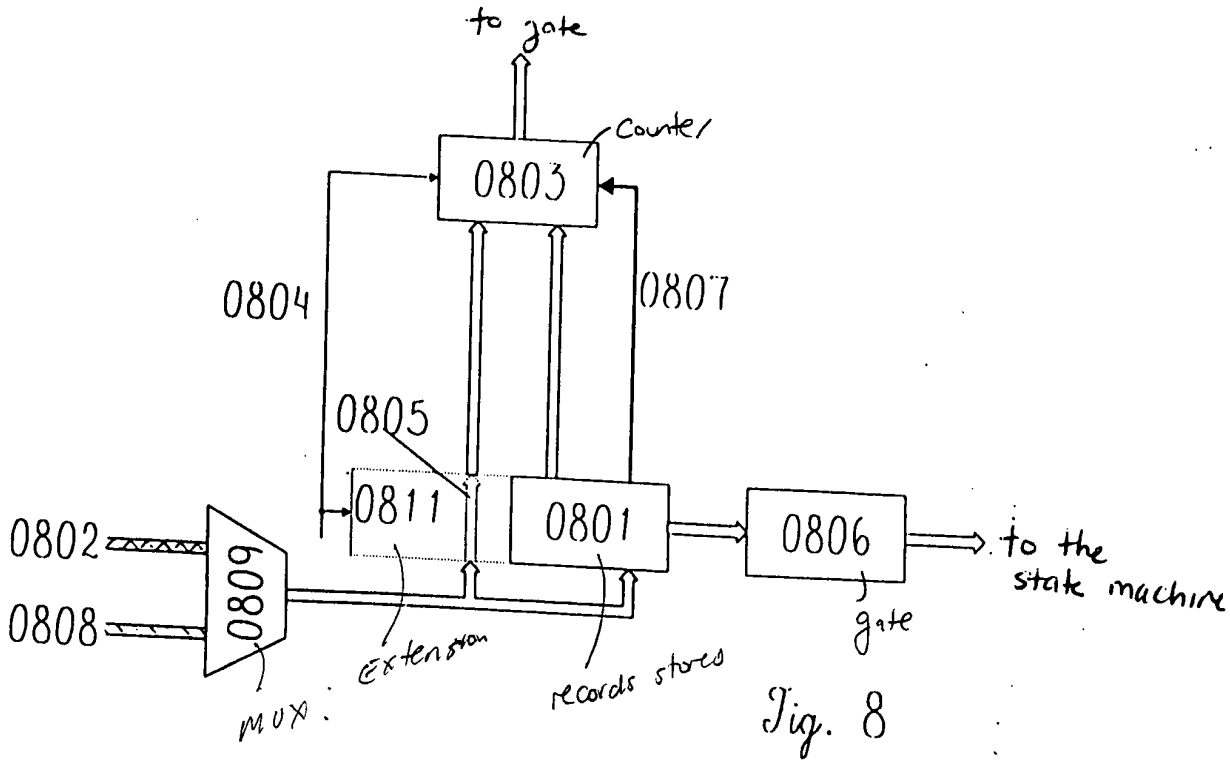
R CLR Q̄
0712
0701
0702
0713
0714
EB Reg

Fig. 7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counter
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0804
0807
0805
0811
0801
0806
to the state machine
0802
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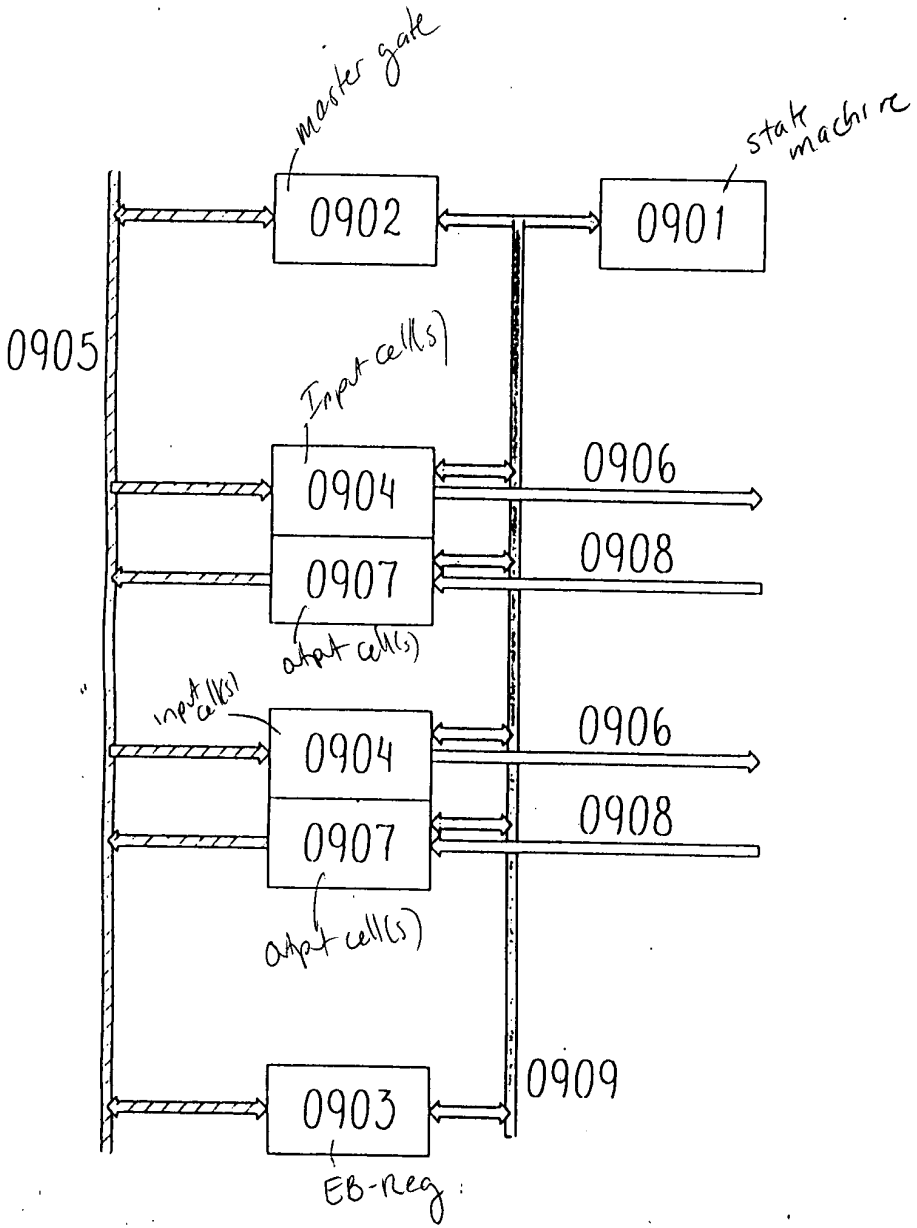
0809
gate
extension
records stores
MUX.

Fig. 8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state machine
0901
0905
Input cell(s)
0904
0906
0907
0908
output cell(s)
input cell(s)
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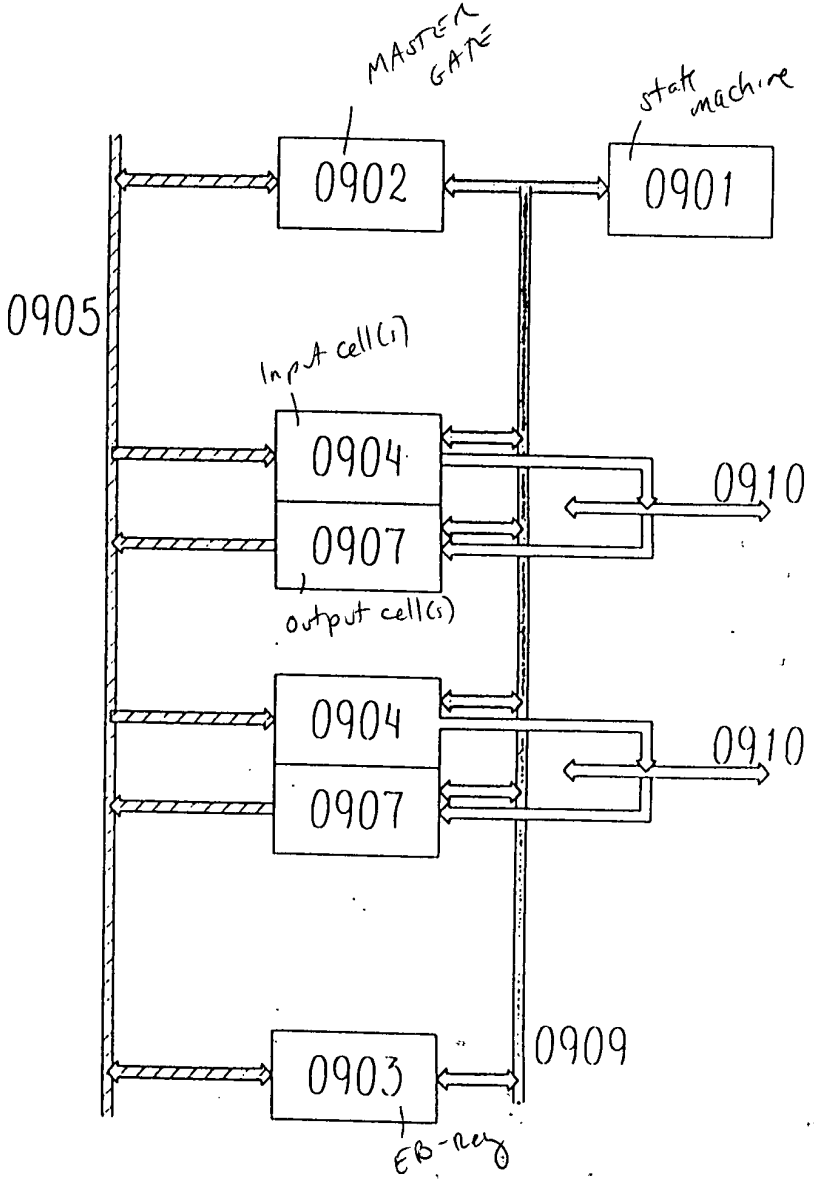
0908
output cell(s)
0909
0903
EB-Reg

Fig. 9a


MASTER GATE
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0905
Input cell(s)
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output cell(s)
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0910
0907
0909
0903
EB-Reg

Fig. 9b

Fig. 10a

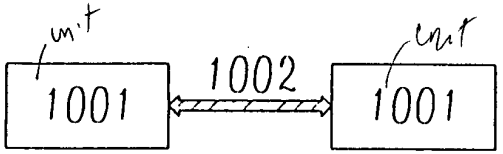


Fig. 10b

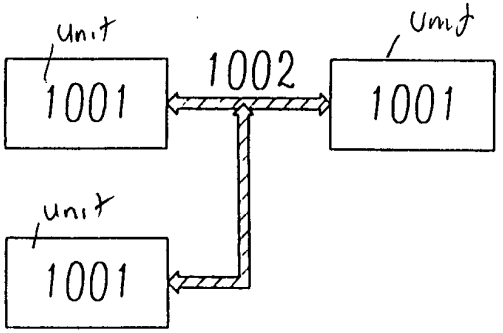


Fig. 10c

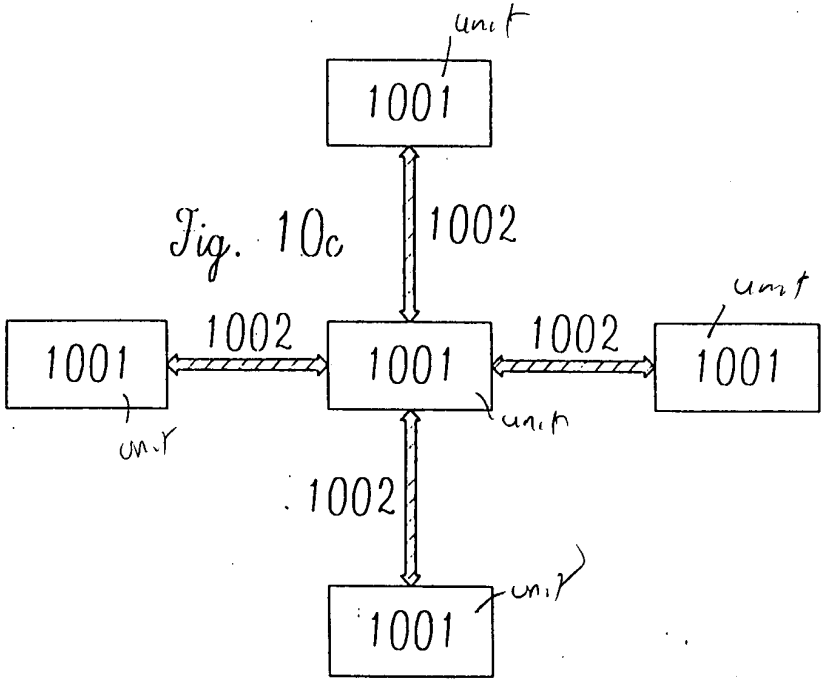


Fig. 10d

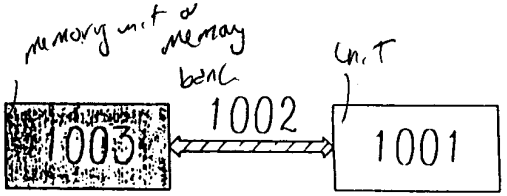


Fig. 10e

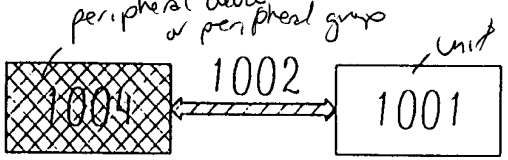


Fig. 10f

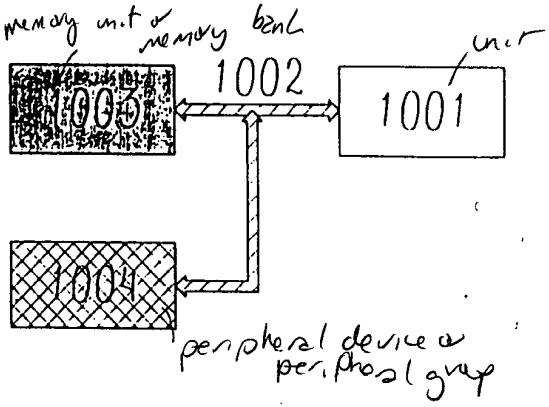
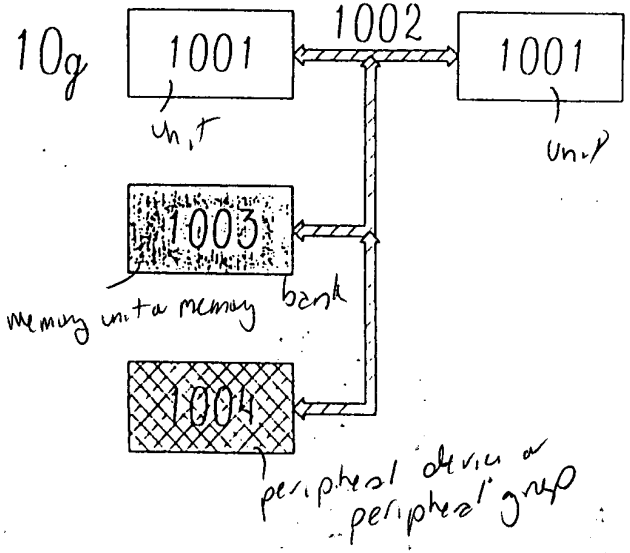
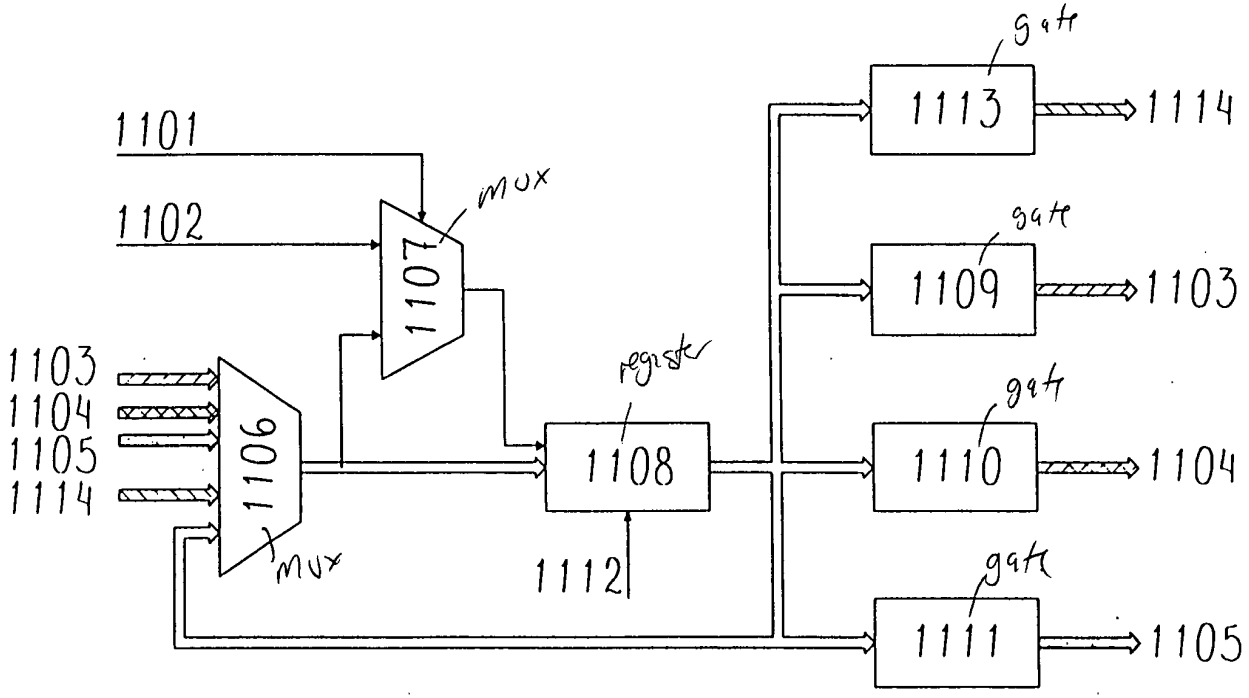


Fig. 10g

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mux
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gate
1104
1111
gate
1105

Fig. 11

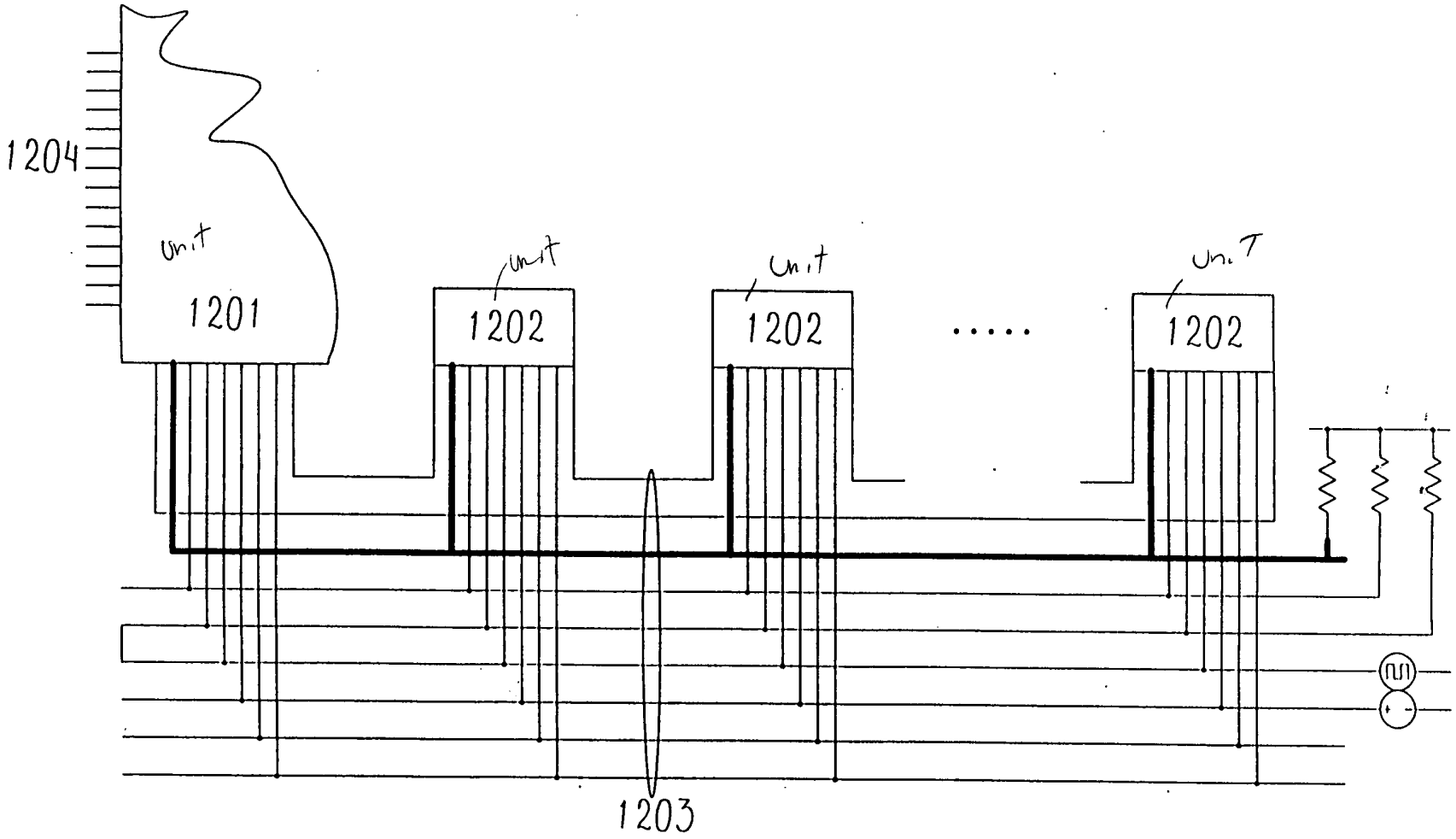

Fig. 12